L Number	Hits	Search Text	DB	Time stamp
1	151	(light adj absorbing) with (via or trench)	USPAT; US-PGPUB	2003/02/20 13:06
2	32	((light adj absorbing) with (via or trench)) and dielectric	USPAT; US-PGPUB	2003/02/20 13:06
3	83	(light adj absorbing) with (via or trench)	EPO; JPO; DERWENT; IBM_TDB	2003/02/20 13:06
4	5	((light adj absorbing) with (via or trench)) and dielectric	EPO; JPO; DERWENT; IBM_TDB	2003/02/20 13:06

DERWENT-ACC-NO: 2000-685874
DERWENT-WEEK: 200067

TITLE: Optical inspection of semiconductor devices by depositing a **light absorbing** layer in the shallow **trench** isolation of silicon on insulator wafer

INVENTOR: LASKY, J B; PHILIPS, B ; SPERANZA, A C ; WONG, J ; YU, M H

PATENT-ASSIGNEE: INT BUSINESS MACHINES CORP[IBMC]

PRIORITY-DATA: 1999US-0224826 (January 4, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6121064 A	September 19, 2000	N/A	008	H01L 021/66

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 6121064A	N/A	1999US-0224826	January 4, 1999

INT-CL (IPC): H01L021/66

ABSTRACTED-PUB-NO: US 6121064A

BASIC-ABSTRACT: NOVELTY - Semiconductor devices are optically inspected by depositing a **light absorbing** layer (20) in the shallow **trench** isolation (STI) of a silicon on insulator (SOI) wafer so that silicon inclusions (4) in the buried insulator layer (2) created during processing of the silicon wafer (3) are blocked during optical inspection of the resulting wafer.

DETAILED DESCRIPTION - Optical inspection of semiconductor devices comprises

providing a material that is capable of masking defects over a semiconductor substrate, and a layer of material to be inspected disposed over this material. Light is emitted through these layers to reflect a portion of any defects of the material layer while attenuating another portion of light the material layer. Any defect in the layer of material is then detected. INDEPENDENT CLAIMS are also included for (A) a method of fabricating and optically inspecting a semiconductor device having an STI comprising depositing a pad **dielectric** layer to a silicon layer (1) of an SOI substrate, patterning and etching a **trench** (25) for an STI in the pad **dielectric** layer and the silicon layer, exposing the first insulative layer (12) within the SOI substrate, growing a thermal oxide film on the walls of the **trench,** depositing a **light absorbing** film on the **trench,** which is then filled with a second insulative material, and inspecting the semiconductor device by (a) emitting light having a wavelength which is absorbed by the silicon layer on the SOI substrate and the **light absorbing** film, and (b) detecting any defects introduced into the STI and subsequently processing of the semiconductor device due to the reflection of the defects; and (B) an optically inspectable semiconductor device having the STI comprising an SOI substrate having a first insulative layer and a single crystal layer of silicon, a pad **dielectric** layer disposed over the silicon layer, an STI etched in the pad **dielectric** layer and silicon layer, a thermal oxide film grown into the **trench, a light absorbing** film deposited on the **trench,** and a second insulative layer to fill the **trench**.

USE - For optically inspecting semiconductor devices.

ADVANTAGE - The method reduces the background defects so that optical
inspection of the SOI wafer is improved without having to discriminate against
the defects created by the STI formation and the inclusions created during
processing. It distinguishes defects created by processing against defects
created in prior level processing so that continual processing may be avoided
prior to correction or removal of defective wafers in the production line.

DESCRIPTION OF DRAWING(S) - The figure shows an elevational partial side view
in cross section of an inspectable SOI wafer having shallow trench isolation.

Silicon layer 1

Buried insulator layer 2

Silicon wafer 3

Silicon inclusions 4

Insulative layer 12

Light absorbing film 20

Trench 25

CHOSEN-DRAWING: Dwg.3/4

TITLE-TERMS:
OPTICAL INSPECT SEMICONDUCTOR DEVICE DEPOSIT LIGHT ABSORB LAYER SHALLOW TRENCH
ISOLATE SILICON INSULATE WAFER

DERWENT-CLASS: L03 S01 S02 S03 U11

CPI-CODES: L04-C12C; L04-C18;

EPI-CODES: S01-G02B1; S02-A03B1; S03-E04F2; U11-C05B5; U11-C05B9C; U11-C08A3;
U11-C08A6; U11-F01A3; U11-F01B4;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2000-208550
Non-CPI Secondary Accession Numbers: N2000-507001

DERWENT-ACC-NO: 1996-039498
DERWENT-WEEK: 199604

TITLE: Binary optical photolithography mask for projecting image onto target
in semiconductor mfr. - having absorber pattern buried below surface of quartz
substrate to provide for max. depth of focus of exposure system without imaging
surface defects and contaminants

INVENTOR: VASUDEV, P K

PATENT-ASSIGNEE: SEMATECH INC[SEMAN]

PRIORITY-DATA: 1994US-0342940 (November 21, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5474865 A	December 12, 1995	N/A	013	G03F 009/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5474865A	N/A	1994US-0342940	November 21, 1994

INT-CL (IPC): G03F009/00

ABSTRACTED-PUB-NO: US 5474865A
BASIC-ABSTRACT: Binary optical photolithography mask (30) for projecting image
pattern onto a target has substrate (31) formed from transparent material
transmitting light in which an absorber pattern (32) formed from light
absorbing material is buried a set distance, d, below the surface near the
target, but not at the surface, for absorbing at least a significant portion of
transmitted light to form an opaque image pattern on the

target. The absorber pattern reflects light scattered from its surface areas back into the substrate at their surface interface and improves image feature definition at the target. The distance, d, at which the absorber pattern is buried below the surface is sufficient to provide for maximum depth of focus of an exposure system within the substrate such that surface defects and contaminants at the surface interface are not imaged onto the target. Also claimed is a method of fabricating the binary optical photolithography mask by forming a photoresistive layer over the substrate, patterning the layer to expose portions of the underlying substrate, etching those exposed portions to a predefined depth to form **trenches** in the substrate, removing the remainder of the photoresistive layer, depositing a layer of **light absorbing** material over the substrate to fill the **trenches**, selectively etching back the layer until only the **trenches** are filled with the **light absorbing** material, and forming a **dielectric** layer of predefined thickness over the substrate and **trenches** to form an upper boundary region of the mask having the **light absorbing** material buried below its surface.

USE - Mask is used for mfr. semiconductor devices.

ADVANTAGE - The buried absorbers in the mask significantly reduce edge diffraction effects and eliminate any need for a pellicle.

CHOSEN-DRAWING: Dwg.5/16

TITLE-TERMS:
BINARY OPTICAL PHOTOLITHOGRAPHIC MASK PROJECT IMAGE TARGET SEMICONDUCTOR MANUFACTURE ABSORB PATTERN BURY BELOW SURFACE QUARTZ SUBSTRATE MAXIMUM DEPTH FOCUS EXPOSE SYSTEM IMAGE SURFACE DEFECT CONTAMINATE

DERWENT-CLASS: L03 P84 U11

CPI-CODES: L04-C06A;

EPI-CODES: U11-C04D; U11-C04E2;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1996-013231
Non-CPI Secondary Accession Numbers: N1996-033328